ARM Cortex™-M0

32-BIT MICROCONTROLLER

NM1820 Series Datasheet

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1 GENERAL DESCRIPTION

The NM1820 series 32-bit microcontroller(MCU) is embedded with ARM® Cortex™-M0 core and monolithic half-bridge gate driver for motor driver applications which require high performance, high integration, and low cost. The Cortex™-M0 is the newest ARM® embedded processor with 32-bit performance at a cost equivalent to the traditional 8-bit microcontroller.

The MCU of NM1820 series can run up to 48 MHz and offers 17.5K-bytes embedded program flash, size configurable data flash (shared with program flash), 2K-byte flash for the ISP, and 2K-byte SRAM. Many system level peripheral functions, such as I/O Port, Timer, UART, SPI, I^2C, ADC, Watchdog Timer, Analog Comparator and Brown-out Detector, have been incorporated into the NM1820 series in order to reduce component count, board space and system cost. These useful functions make the NM1820 series powerful for a wide range of motor driver applications.

The power supply input of NM1820 is up to 40V. The UVLO circuits prevent malfunction when VCC is lower than the specified threshold voltage. It also build-in bootstrap diodes that can reduce output component.

Additionally, the NM1820 series is equipped with ISP (In-System Programming) and ICP (In-Circuit Programming) functions, which allow the user to update the program memory without removing the chip from the actual end product.

2 FEATURES

- Operation Supply Voltage VIN Range from 4.5 to 30V
  - Gate Driver (half-bridge gate drive)
  - 3 low-side and 3 high-side gate drivers
  - More than 0.6A gate driving capability
  - UVLO(Under voltage lockout=4.1V) function to disable PWM output (PWM output low)
  - Embedded two Internal 5V voltage regulators with 35mA driving capability
  - Matched propagation delay of around 500ns for both PWM complementary channels
  - PWM output delay matching < 50 ns
  - Max V_{GS} of Power MOS is up to 5V
  - Thermal shutdown circuitry to limit the junction temperature at 125 ℃
- MCU Core
  - ARM® Cortex™-M0 core running up to 48 MHz
  - One 24-bit system timer
  - Supports Low Power Sleep mode
  - A single-cycle 32-bit hardware multiplier
  - NVIC for the 32 interrupt inputs, each with 4-level of priority
  - Supports Serial Wire Debug (SWD) interface and two watch points/four breakpoints
- Hardware Divider
  - Signed (two's complement) integer calculation
  - 32-bit dividend with 16-bit divisor calculation capacity
  - 32-bit quotient and 32-bit remainder outputs (16-bit remainder with sign extends to 32-bit)
  - Divided by zero warning flag
  - 6 HCLK clocks taken for one cycle calculation
  - Waiting for calculation ready automatically when reading quotient and remainder
- Memory
  - 17.5 KB Flash memory for program memory (APROM)
  - Configurable Flash memory for data memory (Data Flash)
  - 2 KB Flash for loader (LDROM)
  - 2 KB SRAM for internal scratch-pad RAM (SRAM)
- Clock Control
  - 48 MHz internal oscillator (HIRC) (±1% accuracy at 25°C, 5V)
    - Dynamically calibrating the HIRC OSC to 48 MHz ±2% from -40°C to 105°C by external 32.768K crystal oscillator (LXT)

- 10 kHz internal low-power oscillator (LIRC) for Watchdog Timer and Power-down wake-up

- Timer
  - Supports external capture pin (T1EX) for interval measurement
  - Support advanced capture function(P3.0) can continuous capture 4 edge on one signal
  - Provides two channel 32-bit timers. One 8-bit pre-scale counter with 24-bit up counter for each timer
  - Independent clock source for each timer
  - Provides One-shot, Periodic, Toggle and Continuous operation modes
  - 24-bit up counter value is readable through TDR (Timer Data Register)
  - Provides trigger counting/free counting/counter reset function triggered by external capture pin or internal comparator signal
  - Provides event counter function
  - Supports wake-up from Idle or Power-down mode
- PWM
  - Independent 16-bit PWM duty control units with maximum six outputs
  - Supports group/synchronous/independent/ complementary modes
  - Supports One-shot or Auto-reload mode
  - Supports Edge-aligned and Center-aligned type
  - Support Asymmetric mode
  - Programmable dead-zone insertion between complementary channels
  - Each output has independent polarity setting control
  - Hardware fault brake and software brake protections
  - Supports rising, falling, central, period, and fault break interrupts
  - Supports duty/period trigger ADC conversion
  - Timer comparing matching event trigger PWM to do phase change
  - Supports comparator event trigger PWM to force PWM output low for current period
  - Provides interrupt accumulation function
  - Gate driver PWM output by MCU PWM control

MCU PWM Control		Gate Driver PWM Output	
PWM0/2/4	**PWM1/3/5**	**UHO/VHO/WHO**	**ULO/VLO/WLO**
H	L	ON	OFF
L	H	OFF	ON
L	L	OFF	OFF
H	H	OFF	OFF

- WDT (Watchdog Timer)
  - Multiple clock sources

- Supports wake-up from Idle or Power-down mode
- Interrupt or reset selectable on watchdog time-out

- UART (Universal Asynchronous Receiver/Transmitters)
  - Two UART devices
  - Buffered receiver and transmitter, each with 16-byte FIFO for first UART (UART0), each with 4-byte FIFO for second UART (UART1)
  - Programmable baud-rate generator up to 1/16 system clock
- ADC (Analog-to-Digital Converter)
  - 10-bit SAR ADC with 500K SPS
  - Up to 7-ch single-end input and one internal input from band-gap
  - Conversion started either by software trigger, or external pin trigger
  - Supports conversion value monitoring (or comparison) for threshold voltage detection
  - Support sequential mode to continuous conversion 2 channel
- Analog Comparator
  - one analog comparators with programmable 16-level internal voltage reference
  - Build-in CRV (comparator reference voltage)
  - Supports Hysteresis function
  - Interrupt when compared results changed
- I/O Port
  - Up to 10 general-purpose I/O (GPIO) pins for TSSOP-28 package
  - Four I/O modes:
    - Input-only with high impendence
    - Push-pull output
    - Open-drain output
    - Quasi-bidirectional
  - TTL/Schmitt trigger input selectable
  - I/O pin can be configured as interrupt source with edge/level setting
  - Supports high driver and high sink I/O mode
  - Configurable default I/O mode of all pins after POR
- ISP (In-System Programming) and ICP (In-Circuit Programming)
- BOD (Brown-out Detector)
  - With 8 programmable threshold levels: 4.4V/3.7V/3.0V/2.7V/2.4V/2.2V/2.0V/1.7V
  - Supports Brown-out interrupt and reset option
- 96-bit unique ID
- LVR (Low Voltage Reset)
- Operating Temperature: -40℃~105℃

- Reliability: EFT > ± 3.5KV, ESD HBM pass 4KV
- Packages:
  - Green package (RoHS)
  - 28-pin TSSOP

3 PARTS INFORMATION LIST AND PIN CONFIGURATION

3.1 NM1820 Series Product Selection Guide

Part No.	APROM	RAM	Data Flash	ISP Loader ROM	I/O	Timer 32-bit	UART	Comp.	ADC	ISP ICP IAP	IRC 48MHz	Package
NM1820EB0AE	17.5 KB	2 KB	Configurable	2 KB	up to 10	2x 32-bit	2	2	7 x10-bit	v	v	TSSOP 28pin
NM1820LB0AE	17.5 KB	2 KB	Configurable	2 KB	up to 30	2x 32-bit	2	2	12 x10-bit	v	v	LQFP 48pin

Table 3.1-1 NM1820 Series Product Selection Guide

3.2 PIN CONFIGURATION

3.2.1 TSSOP 28-pin

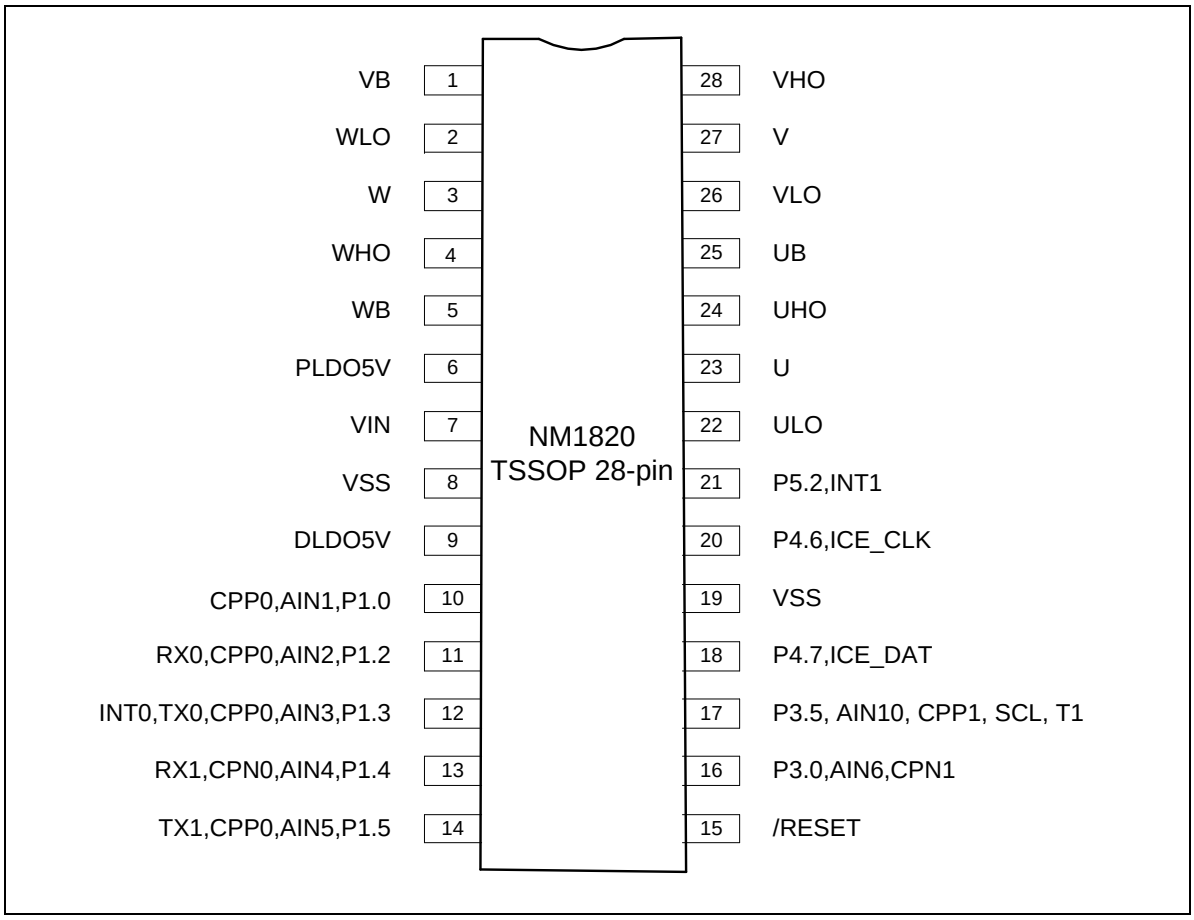


Figure 3.2-1 NM1820 Series TSSOP 28-pin Diagram

3.3 Pin Description

Pin Number TSSOP 28-pin	Pin Name	Pin Type	Description
1	VB	HP	V-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and V.
2	WLO	HO	Output for W-phase low-side MOSFET. Connect to W-phase low-side MOSFET gate.
3	W	HI	W-Phase input. It should be connected to high-side MOSFET source and low-side FET drain.
4	WHO	HO	Output for W-phase high-side MOSFET. Connect to W-phase high-side MOSFET gate.
5	WB	HP	W-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and W.
6	PLDO5V	P	5V LDO OUT. Recommend connect a capacitor to GND.
7	VIN	HP	Power supply for internal control circuit. Recommend connect a capacitor to GND to stable the input power.
8	VSS	P	Ground pin for digital circuit
9	DLDO5V	P	5V LDO OUT for digital device. Recommend connect a capacitor to GND.
10	P1.0	I/O	General purpose digital I/O pin
	AIN1	AI	ADC analog input pin
	ACMP0_P	AI	Analog comparator positive input pin
11	P1.2	I/O	General purpose digital I/O pin
	AIN2	AI	ADC analog input pin
	RX	I	UART data receiver input pin
	ACMP0_P	AI	Analog comparator positive input pin
12	P1.3	I/O	General purpose digital I/O pin
	AIN3	AI	ADC analog input pin
	TX	O	UART transmitter output pin
	ACMP0_P	AI	Analog comparator positive input pin
	INT0	I	External interrupt 0 input pin
13	P1.4	I/O	General purpose digital I/O pin
	AIN4	I/O	ADC analog input pin
	ACMP0_N	AI	Analog comparator negative input pin
	RX1	I	UART1 data receiver input pin
14	P1.5	I/O	General purpose digital I/O pin
	AIN5	AI	ADC analog input pin
	ACMP0_P	AI	Analog comparator positive input pin
	TX1	O	UART1 transmitter output pin
15	/RESET	I(ST)	The Schmitt trigger input pin for hardware device reset.

			/RESET pin has an internal pull-up resistor allowing power-on reset by simply connecting an external capacitor to GND.
16	**P3.0**	**I/O**	General purpose digital I/O pin
	AIN6	**AI**	ADC analog input pin
	ACMP1_N	**AI**	Analog comparator negative input pin
17	**P3.5**	**I/O**	General purpose digital I/O pin
	TM1	**I/O**	Timer 1 external event counter input pin
	SCL	**I/O**	I2C clock I/O pin
	ACMP1_P	**AI**	Analog comparator positive input pin
	AIN10	**AI**	ADC analog input pin
18	**P4.7**	**I/O**	General purpose digital I/O pin
	ICE_DAT	**I/O**	Serial wired debugger data pin
19	**VSS**	**P**	Ground pin for digital circuit
20	**P4.6**	**I/O**	General purpose digital I/O pin
	ICE_CLK	**I**	Serial wired debugger clock pin
21	**P5.2**	**I/O**	General purpose digital I/O pin
	INT1	**I**	External interrupt 1 input pin
22	**ULO**	**HO**	Output for U-phase low-side MOSFET. Connect to U-phase low-side MOSFET gate.
23	**U**	**HI**	U-Phase input. It should be connected to U-phase high-side MOSFET source and low-side FET drain.
24	**UHO**	**HO**	Output for U-phase high-side MOSFET. Connect to U-phase high-side MOSFET gate.
25	**UB**	**HP**	U-phase high-side bootstrap supply. External bootstrap capacitor is required. Connect bootstrap capacitor across this pin and U.
26	**VLO**	**HO**	Output for V-phase low-side MOSFET. Connect to V-phase low-side MOSFET gate.
27	**V**	**HI**	V-Phase input. It should be connected to V-phase high-side MOSFET source and low-side FET drain
28	**VHO**	**HO**	Output for V-phase high-side MOSFET. Connect to V-phase high-side MOSFET gate.

[1] Low voltage I/O type description. I: input, O: output, I/O: quasi bi-direction, D: open-drain, P: power pin, ST: Schmitt trigger, A: Analog input.

[2] High voltage I/O type description. HI: input, HO: output, HP: power pin.

4 BLOCK DIAGRAM

4.1 NM1820 Block Diagram

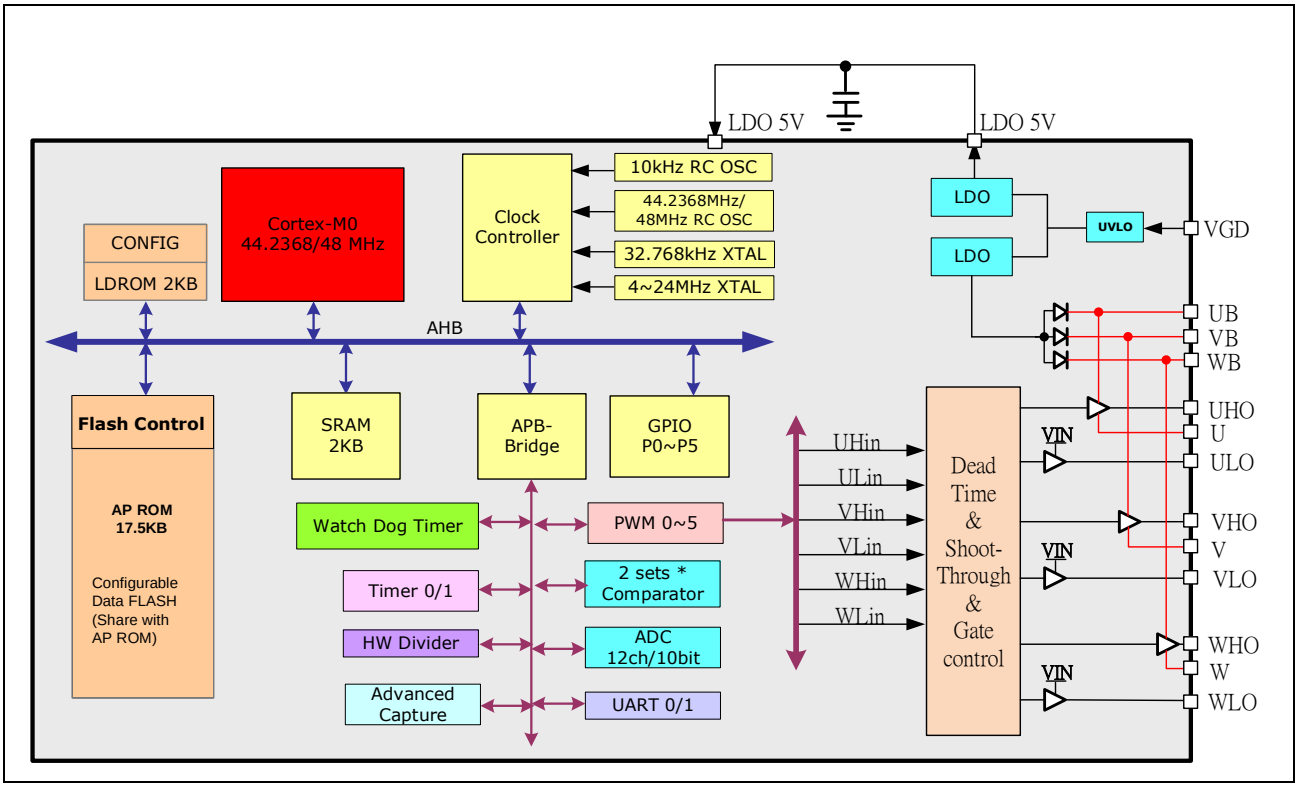
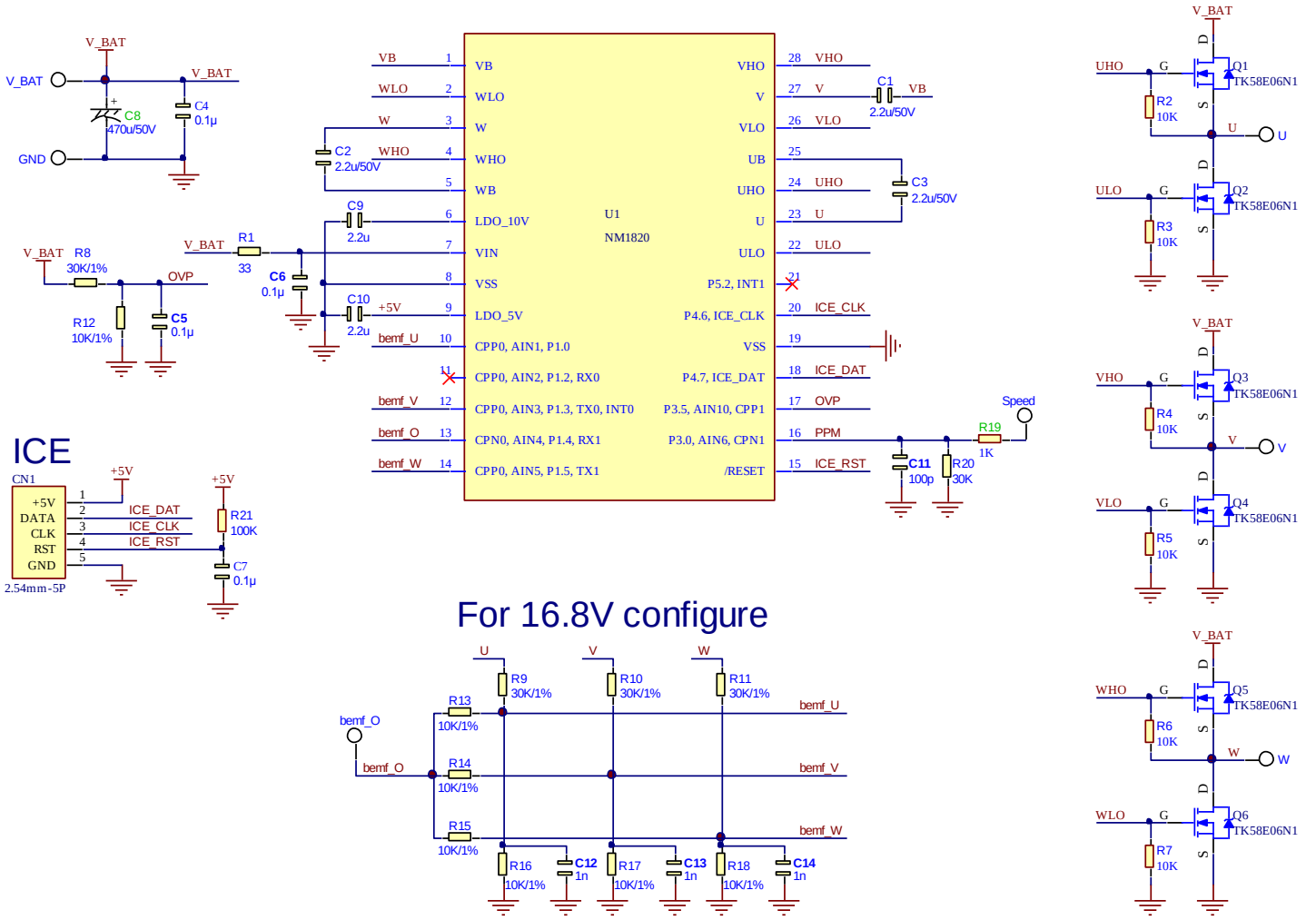


Figure 4.1-1 NM1820 Series Block Diagram

5 APPLICATION CIRCUIT FOR SENSORLESS CONTROL



6 NM1820 ELECTRICAL CHARACTERISTICS

6.1 Absolute Maximum Ratings

Parameter		Min	Max	Unit
VIN Power Supply		-0.3	30	V
Low voltage I/O pins		-0.3	LDO5V+0.3	V
High voltage I/O pins		-0.3	40	V
Oscillator Frequency		4	24	MHz
Maximum Current into V_{DD}		-	120	mA
Maximum Current out of V_{SS}		-	120	mA
Maximum Current sunk by an low voltage I/O pin		-	35	mA
Maximum Current sourced by an low voltage I/O pin		-	35	mA
Maximum Current sunk by total low voltage I/O pins		-	100	mA
Maximum Current sourced by total low voltage I/O pins		-	100	mA
Supply Output Pulse Current (10ms)			2.5	A
Thermal Resistance, θ_{JA}			40	℃/W
Thermal Resistance, θ_{JC}			10	℃/W
Operating Temperature		-40	105	℃
Storage Temperature		-55	150	℃
ESD Protection	Human Body Mode		4	KV
	Machine Mode		200	V
	Latch-up		100	mA

Note: Exposure to conditions beyond those listed under absolute maximum ratings may adversely affects the life and reliability of the device.

6.2 DC Electrical Characteristics

6.2.1 DC Electrical Characteristic for MCU

(V_{DD} - V_{SS} = 2.5 ~ 5.5 V, T_A = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{DD}	Input power voltage of MCU	2.5	-	LDO5V+0.3	V	V_{DD} = 2.5V ~ 5.5V up to 48 MHz
V_{DD}	Input power voltage of MCU	-0.3	-	-	V	
I_{DD1}	MCU Operating Current Normal Run Mode HCLK = 48MHz while(1){} Executed from Flash	-	17	-	mA	V_{DD} = 5.5V; Internal RC48M = Enable; All digital modules = Enabled
I_{IDLE1}	Operating Current Idle Mode HCLK = 48MHz		10		mA	VDD = 5.5V, PLL on, All digital module on
			5		mA	VDD = 5.5V, PLL on, All digital module off
I_{PWD1}	Standby Current Power-down Mode (Deep Sleep Mode)		1.5		μA	V_{DD} = 5.5 V, All oscillators and analog blocks turned off.
I_{LK}	Input Leakage Current P1/3/4	-1	-	+1	μA	V_{DD} = 5.5 V, 0 < V_{IN} < V_{DD} Open-drain or input only mode
V_{IL1}	Input Low Voltage P1/3/4 (TTL Input)	-0.3	-	0.8	V	V_{DD} = 4.5 V
		-0.3	-	0.6		V_{DD} = 2.5 V
V_{IH1}	Input High Voltage P1/3/4 (TTL Input)	2.0	-	V_{DD} + 0.3	V	V_{DD} = 5.5 V
		1.5	-	V_{DD} + 0.3		V_{DD} = 3.0 V
V_{ILS}	Negative-going Threshold (Schmitt Input), nRST	-0.3	-	0.3 V_{DD}	V	-
V_{IHS}	Positive-going Threshold (Schmitt Input), nRST	0.7 V_{DD}	-	V_{DD} + 0.3	V	-
R_{RST}	Internal nRST Pin Pull-up Resistor	17.5		150	kΩ	V_{DD} = 2.1 V ~ 5.5V
T_{SD}	Thermal Shutdown Temperature		165		℃	Thermal Protection
T_{SDHYS}	Thermal Shutdown Hysteresis		50		℃	Thermal Protection

Notes:

1. Pins of P0, P1, P2, P3 and P4 can source a transition current when they are being externally driven from 1 to 0. In the condition of V_{DD}=5.5V, the transition current reaches its maximum value when pin voltage approximates to 2V.

6.2.2 DC Electrical Characteristic for Gate Driver

(-40℃ < TJ < 85℃, and recommended supply voltage unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Supply voltage						
VIN	Vpower		6		30	V
VIN Under Voltage Lockout	UVLO	VIN Falling			4.1	V
V IN Under Voltage Hysteresis				0.4		V
VIN standby current		At VIN < 4.1V		10		uA
Gate Driver Output						
PWM input to output delay	T_{I2O}			500		ns
PWM output matching	T_{MATCH}			50		ns
PWM output low to high	I_{PWM_HI}	At VIN=8V	0.6			A
PWM output high to low	I_{PWM_LO}	At VIN=8V	0.6			A
Internal 5V regulator (LDO5V)						
Output Current	I_{OUT}	At VIN>8V		35		mA
SLEEP Current	I_{STB}	VIN < 4.1V		10		mA
Output Voltage		At VIN>8V	-5%	5	5%	V
Internal 5V regulator (LDO5V) For Gate driver						
Output Current	I_{OUT}	At VIN>12V		35		mA
SLEEP Current	I_{STB}	At VIN < 4.1V		1		mA
Operation Voltage	VLDO	At VIN>12V	-5%	10	+5%	V
LDO dropped volt	V_{DROP}	From VIN to LDO10V output		1		V
Thermal Protection						
Thermal Shutdown Temperature	TSD			165		℃
Thermal Shutdown Hysteresis	TSDHYS			50		℃
Thermal Warning Temperature	TWRN			130		℃

6.3 AC Electrical Characteristics

6.3.1 48 MHz Internal High Speed RC Oscillator (HIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{HRC}	Supply Voltage	1.62	1.8	1.98	V	-
f_{HRC}	Center Frequency	-	48		MHz	-
	Calibrated Internal Oscillator Frequency	-1	-	+1	%	T_A = 25 ℃ V_{DD} = 5 V
		-3(1)	-	+3(1)	%	T_A = -40 ℃ ~ 105 ℃ V_{DD} = 2.1 V ~ 5.5 V
I_{HRC}	Operating Current	-		-	μA	T_A = 25 ℃,V_{DD} = 5 V

6.3.2 10 kHz Internal Low Speed RC Oscillator (LIRC)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
V_{LRC}	Supply Voltage	2.5	-	5.5	V	-
f_{LRC}	Center Frequency	-	10	-	kHz	
	Oscillator Frequency	-50	-	+50	%	V_{DD} = 2.1 V ~ 5.5 V T_A = -40℃ ~ +105℃

6.3.3 Comparator

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{CMP}	Supply Voltage	2.1	-	5.5	V	
T_A	Temperature	-40	25	105	℃	-
I_{CMP}	Operation Current	-	40	80	μA	V_{DD5V} = 5 V
V_{OFF}	Input Offset Voltage		10	20	mV	-
V_{SW}	Output Swing	0.1	-	AV_{DD} - 0.1	V	-
V_{COM}	Input Common Mode Range	0.1	-	AV_{DD} – 0.1	V	-
-	DC Gain		60	-	dB	-
T_{PGD}	Propagation Delay	-	200	-	ns	V_{COM} = 1.2 V, V_{DIFF} = 0.1 V
V_{HYS}	Hysteresis	-	±30		mV	V_{COM} = 1.2 V
T_{STB}	Stable time	-	-	1.2	μs	

6.3.4 10-bit SAR ADC

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
-	Resolution	-	-	10	Bit	-
DNL	Differential Nonlinearity Error	-	-1~1.5	-1~+3	LSB	-
INL	Integral Nonlinearity Error	-	±1	±2	LSB	-
E_O	Offset Error	-	1	2	LSB	-
E_G	Gain Error (Transfer Gain)	-	-1	-1.5	LSB	-
E_A	Absolute Error	-	3	5	LSB	-
-	Monotonic	Guaranteed			-	-
F_{ADC}	ADC Clock Frequency	-	-	8	MHz	V_{DD5V} = 4.5~5.5 V
		-	-	5.4		V_{DD5V} = 2.1~5.5 V
F_S	Sample Rate (F_{ADC}/T_{CONV})	-	-	500	kSPS	V_{DD5V} = 4.5~5.5 V
		-	-	300	kSPS	V_{DD5V} = 2.1~5.5 V
T_{ACQ}	Acquisition Time (Sample Stage)	N+1			$1/F_{ADC}$	N is sampling counter, N=0,1,2, 4,8, 16,32, 4, 128, 256,1024
T_{CONV}	Total Conversion Time	N+14			$1/F_{ADC}$	
I_{DDA}	Supply Current (Avg.)	-	200	-	μA	V_{DD5V} = 5.5 V
V_{DD}	Analog Input Voltage	0	-	V_{DD5V}	V	-
C_{IN}	Input Capacitance	-	12	-	pF	-
R_{IN}	Input Load	-	7	-	kΩ	-

Note: ADC voltage reference is same with AV_{DD}

6.3.5 Power-on Reset

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
V_{POR}	Reset Voltage		1.25		V	-

6.3.6 Brown-out Detector

Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
T_A	Temperature	-40	25	105	℃	-
I_{BOD}	Quiescent Current		100		μA	V_{DD5V} = 5.5 V
V_{BOD}	Brown-out Voltage		4.3		V	BOV_VL [2:0] = 3
			3.7		V	BOV_VL [2:0] = 2
			3.0		V	BOV_VL [2:0] = 7
			2.7		V	BOV_VL [2:0] = 1
			2.4		V	BOV_VL [2:0] = 6
			2.2		V	BOV_VL [2:0] = 0
			2.0		V	BOV_VL [2:0] = 5
			1.7		V	BOV_VL [2:0] = 4

6.3.7 Flash DC Electrical Characteristics

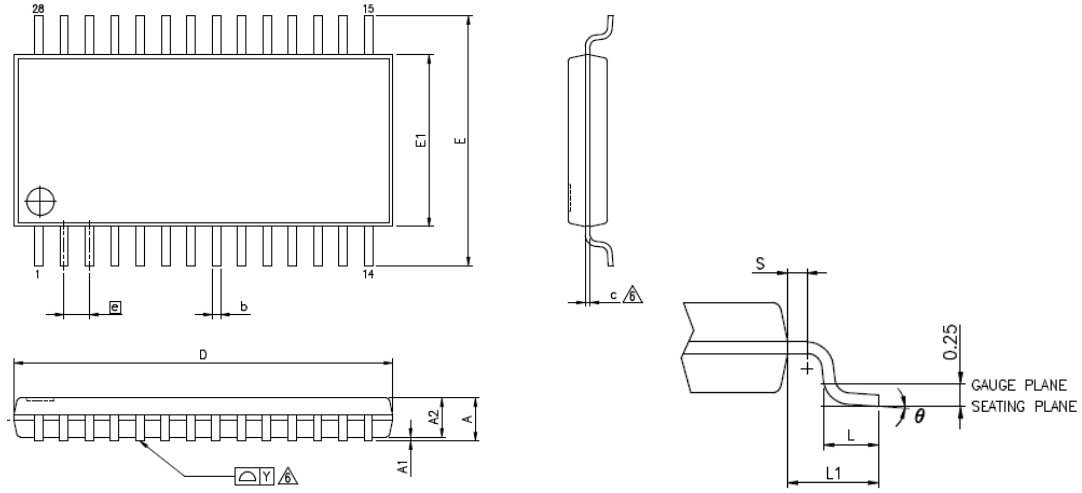
Symbol	Parameter	Min	Typ	Max	Unit	Test Condition
V_{FLA}[2]	Supply Voltage	1.62	1.8	1.98	V	
N_{ENDUR}	Endurance	-	-	20,000	cycles[1]	
T_{RET}	Data Retention	10	-	-	year	T_A = 85℃
T_{ERASE}	Sector Erase Time	-	6	-	ms	
T_{PROG}	Program Time	-	7.5	-	us	
I_{DD1}	Read Current	-	4	-	mA	
I_{DD2}	Program Current	-	3.5	-	mA	
I_{DD3}	Erase Current	-	2	-	mA	

Notes:

1. Number of program/erase cycles.
2. V_{FLA} is source from chip LDO output voltage.
3. Guaranteed by design, not test in production.

7 PACKAGE DIMENSION

7.1 28-pin (4.4mm x 9.7mm)



VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.20
A1	0.00	–	0.15
A2	0.80	1.00	1.05
b	0.19	–	0.30
c	0.09	–	0.20
D	9.60	9.70	9.80
E1	4.30	4.40	4.50
E	6.40 BSC		
e	0.65 BSC		
L1	1.00 REF		
L	0.45	0.60	0.75
S	0.20	–	–
θ	0°	–	8°
Y	0.10		

8 REVISION HISTORY

Revision	Date	Description
0.1	May. 07, 2015	Preliminary version
0.4	February 2, 2016	Revise the table of “Gate driver PWM output by MCU PWM control”.
0.5	June 17, 2016	Revise the Part Number, and package information.
0.6	June 20, 2016	Modify “APPLICATION CIRCUIT”
0.7	Sept 19, 2016	Modify pin6 and pin9 description

Important Notice

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